



Description

JMG N-channel Enhancement Mode Power MOSFET

Features

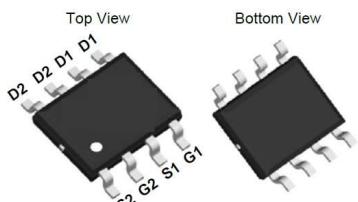
- 100V,4.5A
- $R_{DS(ON)} < 62\text{m}\Omega$ @ $V_{GS} = 10\text{V}$
- $R_{DS(ON)} < 90\text{m}\Omega$ @ $V_{GS} = 4.5\text{V}$
- Advanced Split Gate Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

Application

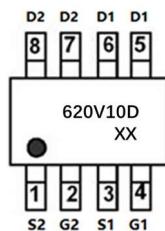
- Load Switch
- PWM Application
- Power management



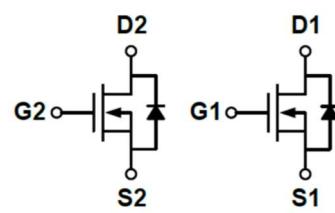
100% UIS TESTED!
100% ΔV_{ds} TESTED!



SOP-8(dual chip)



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
620V10D	JMGP620V10D	TAPING	SOP-8	13inch	4000	48000

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Max.	Units
V_{DSS}	Drain-Source Voltage	100	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_A = 25^\circ\text{C}$	A
		$T_A = 100^\circ\text{C}$	A
I_{DM}	Pulsed Drain Current ^{note1}	18	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}	4.2	mJ
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	W
$R_{\theta JA}$	Thermal Resistance, Junction to Case		$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

**Electrical Characteristics** ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=100\text{V}, V_{GS}=0\text{V}$,	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1	2	3	V
$R_{DS(\text{on})}$ note3	Static Drain-Source on-Resistance	$V_{GS}=10\text{V}, I_D=3.5\text{A}$	-	47	62	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=2\text{A}$	-	60	90	
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=50\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	-	429.4	-	pF
C_{oss}	Output Capacitance		-	58.3	-	pF
C_{rss}	Reverse Transfer Capacitance		-	2.9	-	pF
Q_g	Total Gate Charge	$V_{DS}=50\text{V}, I_D=5\text{A}, V_{GS}=10\text{V}$	-	7.6	-	nC
Q_{gs}	Gate-Source Charge		-	1.4	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	2.4	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=50\text{V}, I_D=5\text{A}, R_{\text{GEN}}=2\Omega, V_{GS}=10\text{V}$	-	15.6	-	ns
t_r	Turn-on Rise Time		-	4.2	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	26.8	-	ns
t_f	Turn-off Fall Time		-	3.6	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	4.5	-	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	18	-	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}, I_s=5\text{A}$	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	$I_F=5\text{A}, dI/dt=100\text{A}/\mu\text{s}$	-	36.1	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	50.4	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J=25^\circ\text{C}, VDD=50\text{V}, VG=10\text{V}, RG=25\Omega, L=0.3\text{mH}, IAS=5.3\text{A}$ 3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

Typical Performance Characteristics

Figure 1: Output Characteristics

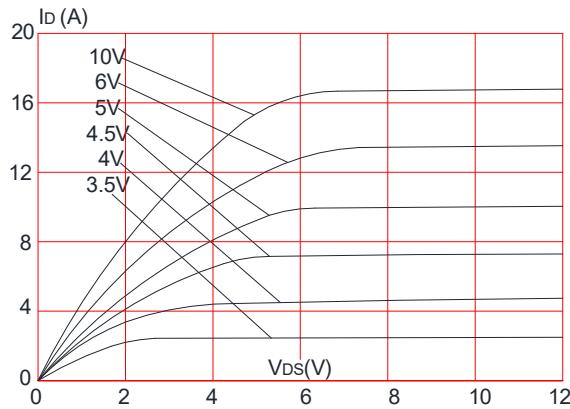


Figure 3: On-resistance vs. Drain Current

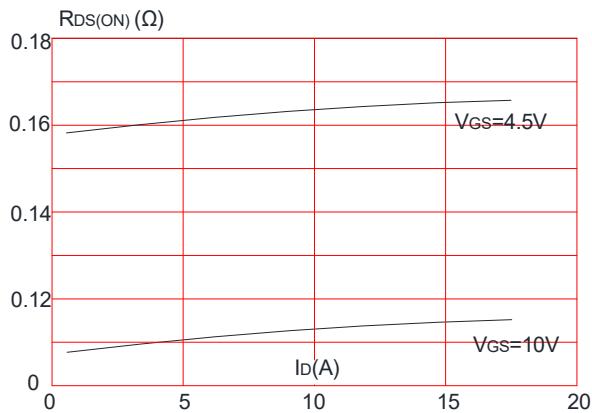


Figure 5: Gate Charge Characteristics

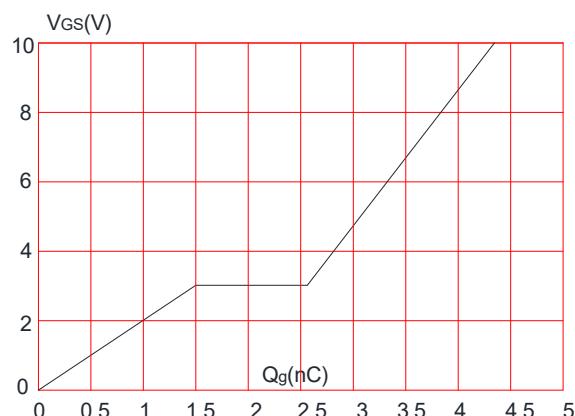


Figure 2: Typical Transfer Characteristics

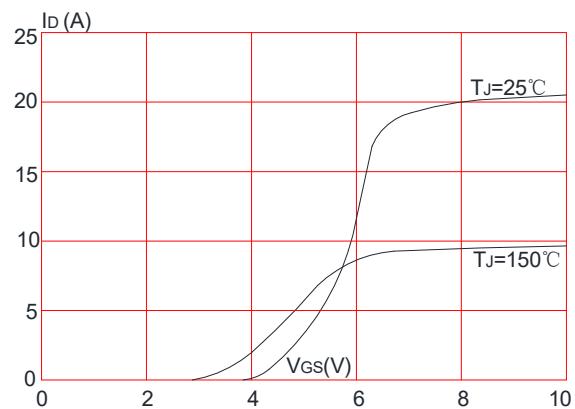


Figure 4: Body Diode Characteristics

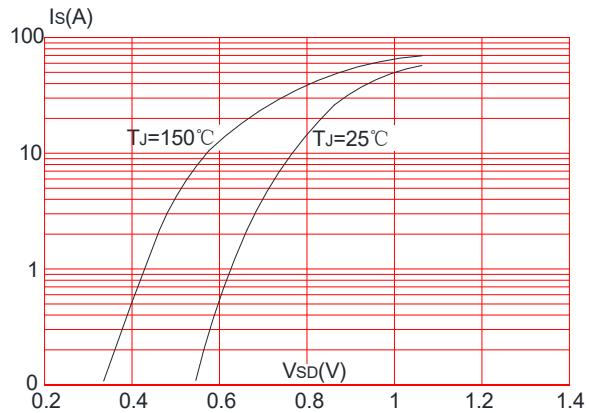


Figure 6: Capacitance Characteristics

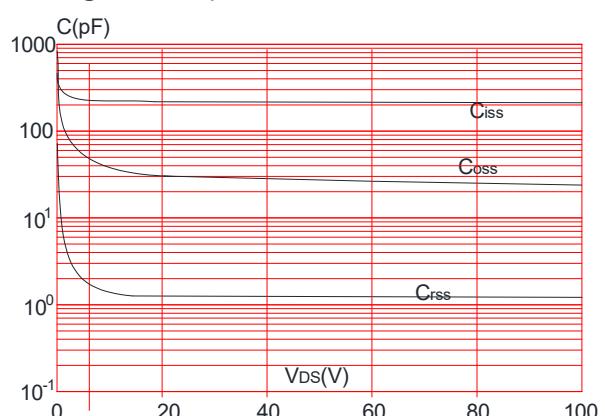


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

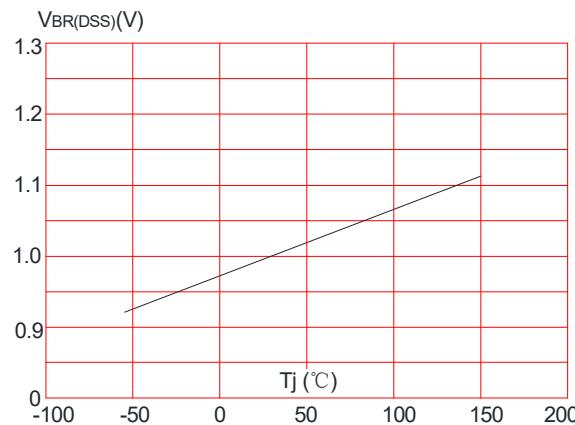


Figure 9: Maximum Safe Operating Area

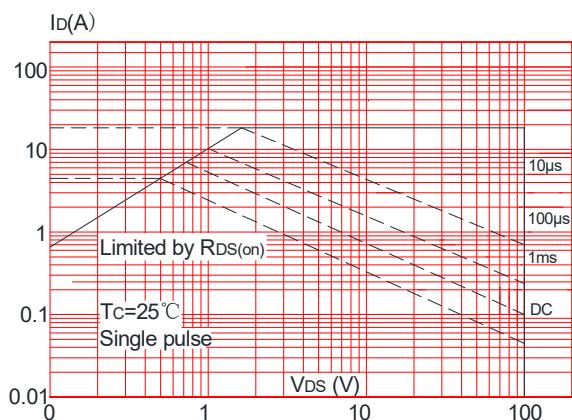


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

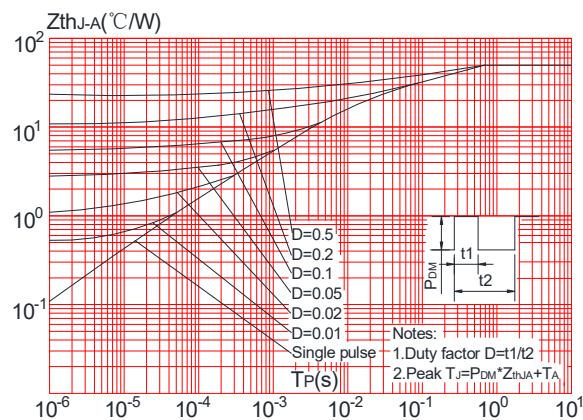


Figure 8: Normalized on Resistance vs. Junction Temperature

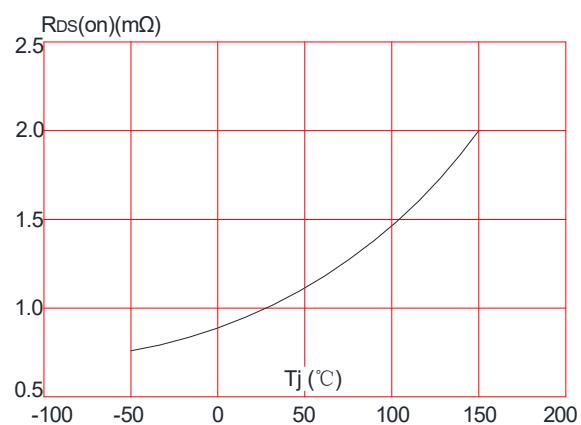
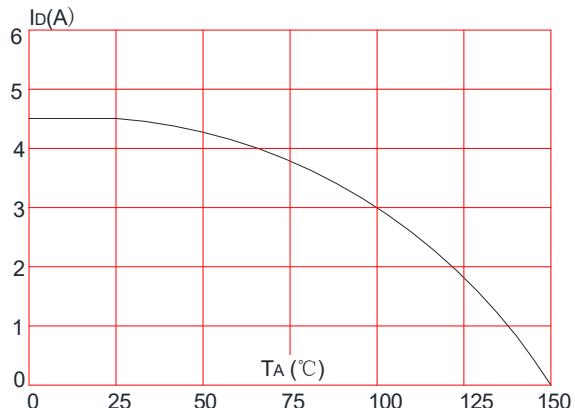


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature



Test Circuit

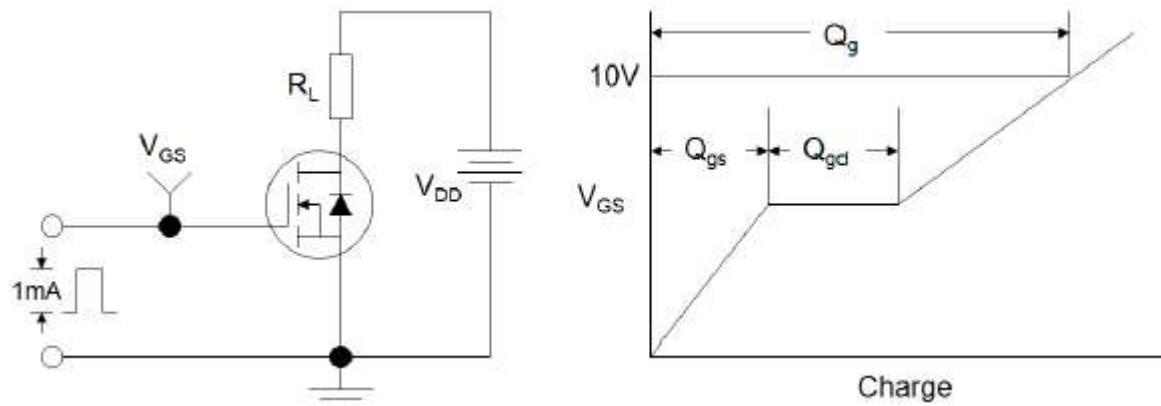


Figure1:Gate Charge Test Circuit & Waveform

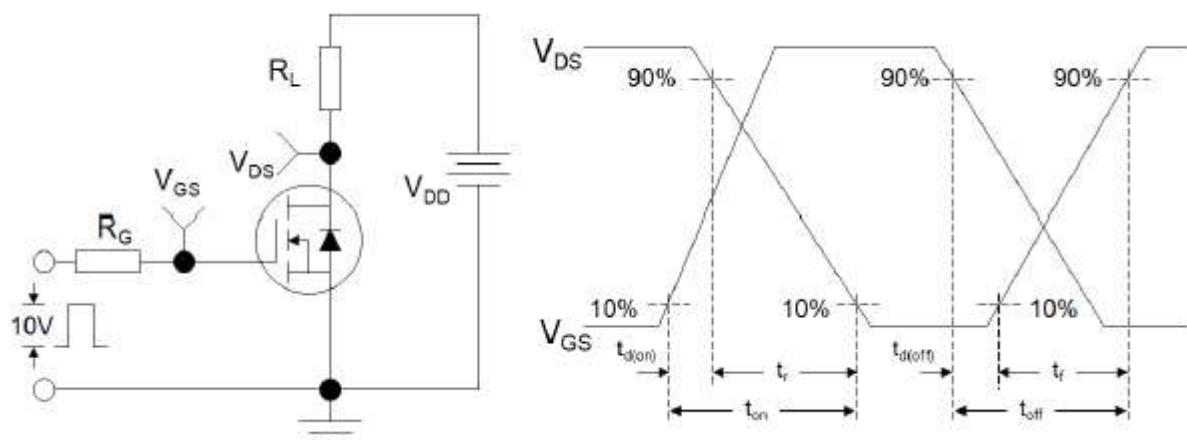


Figure 2: Resistive Switching Test Circuit & Waveforms

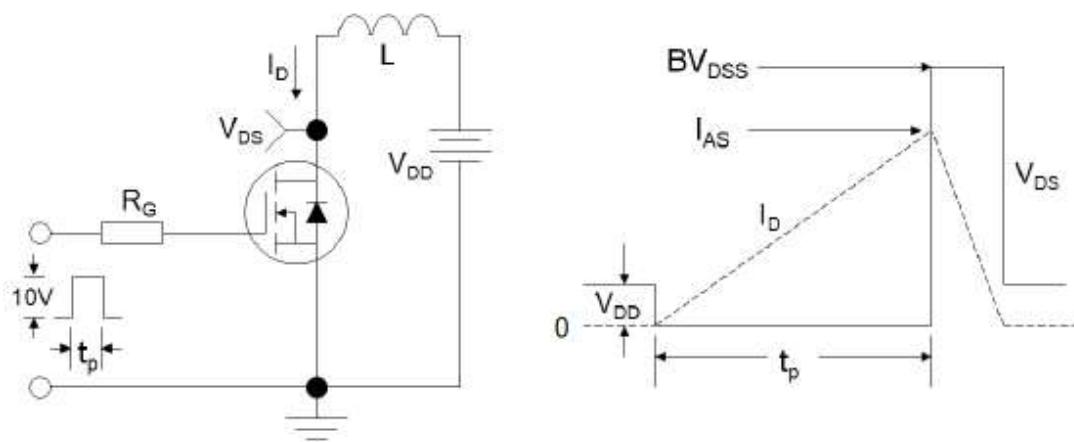
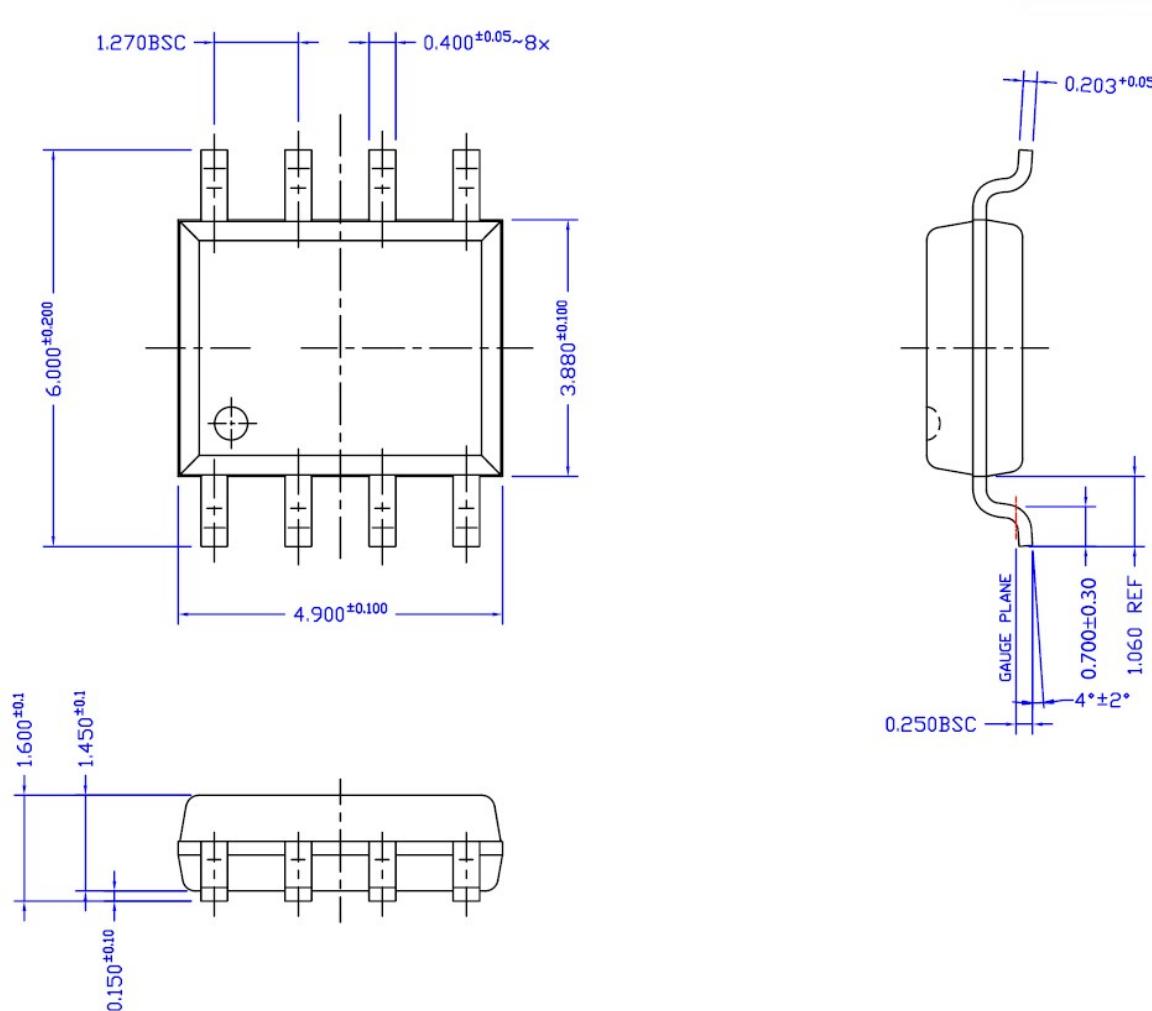


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



Package Mechanical Data-SOP-8



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