Description

JMG N-channel Enhancement Mode Power MOSFET

Features

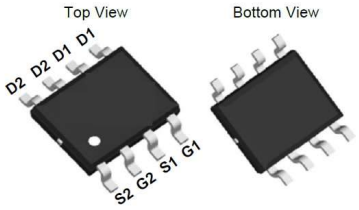
- 100V,4.5A
  $R_{DS(ON)}$< 62mΩ @ V_{GS}=10V
  $R_{DS(ON)}$< 90mΩ @ V_{GS}=4.5V
- Advanced Split Gate Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

Application

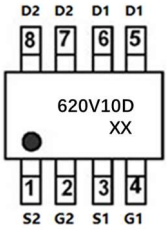
- Load Switch
- PWM Application
- Power management

RoHS

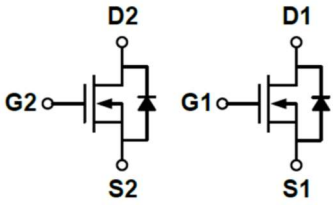
100% UIS TESTED!
100% ΔVds TESTED!



SOP-8(dual chip)



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
620V10D	JMGP620V10D	TAPING	SOP-8	13inch	4000	48000

Absolute Maximum Ratings (T_A=25℃ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		100	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current	T_A= 25℃	4.5	A
		T_A= 100℃	3	A
I_{DM}	Pulsed Drain Current note1		18	A
E_{AS}	Single Pulsed Avalanche Energy note2		4.2	mJ
P_D	Power Dissipation	T_A= 25℃	2.5	W
$R_{\theta JA}$	Thermal Resistance, Junction to Case		50	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Electrical Characteristics (T_J=25℃ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V,I_D=250μA	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =100V, V_{GS} = 0V,	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	V_{DS} =0V,V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250μA	1	2	3	V
$R_{DS(on)}$	Static Drain-Source on-Resistance note3	V_{GS} =10V, I_D =3.5A	-	47	62	mΩ
		V_{GS} =4.5V, I_D =2A	-	60	90	
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} =50V, V_{GS} =0V, f = 1MHz	-	429.4	-	pF
C_{oss}	Output Capacitance		-	58.3	-	pF
C_{rss}	Reverse Transfer Capacitance		-	2.9	-	pF
Q_g	Total Gate Charge	V_{DS} =50V, I_D =5A, V_{GS} =10V	-	7.6	-	nC
Q_{gs}	Gate-Source Charge		-	1.4	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	2.4	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=50V, I_D=5A, R_{GEN}=2Ω, V_{GS} =10V	-	15.6	-	ns
t_r	Turn-on Rise Time		-	4.2	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	26.8	-	ns
t_f	Turn-off Fall Time		-	3.6	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	4.5	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	18	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_S=5A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	I_F=5A,dI/dt=100A/μs	-	36.1	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	50.4	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: T_J=25℃,VDD=50V,VG=10V, RG=25Ω, L=0.3mH,IAS=5.3A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

Typical Performance Characteristics

Figure1: Output Characteristics

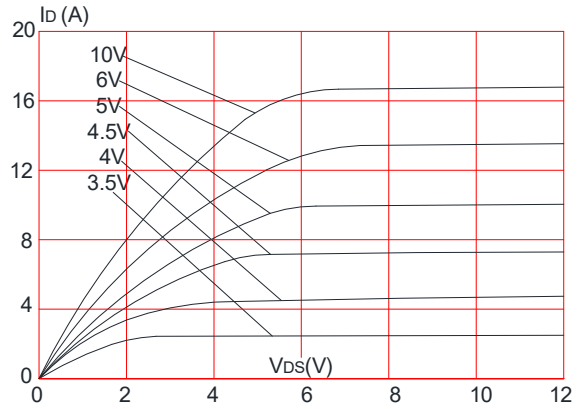


Figure 2: Typical Transfer Characteristics

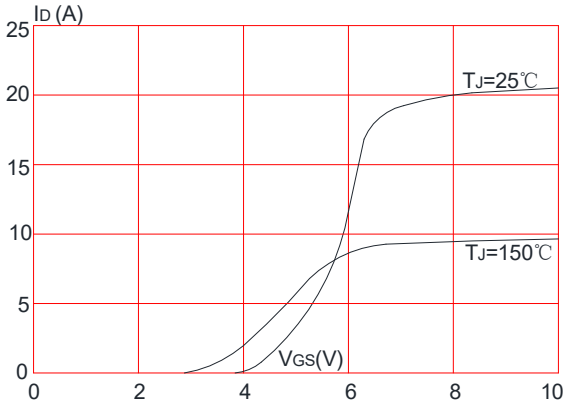


Figure 3: On-resistance vs. Drain Current

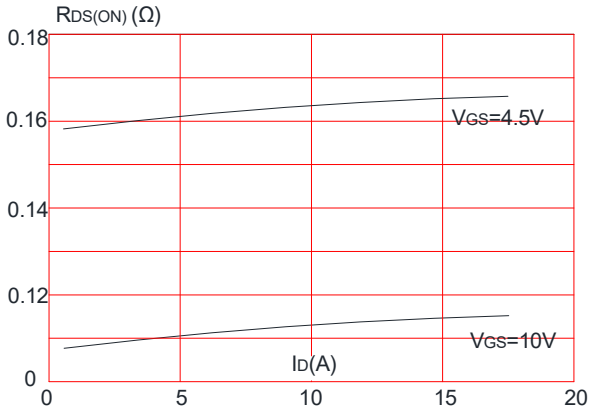


Figure 4: Body Diode Characteristics

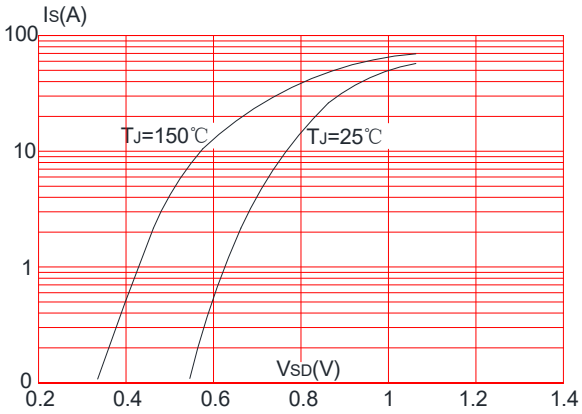


Figure 5: Gate Charge Characteristics

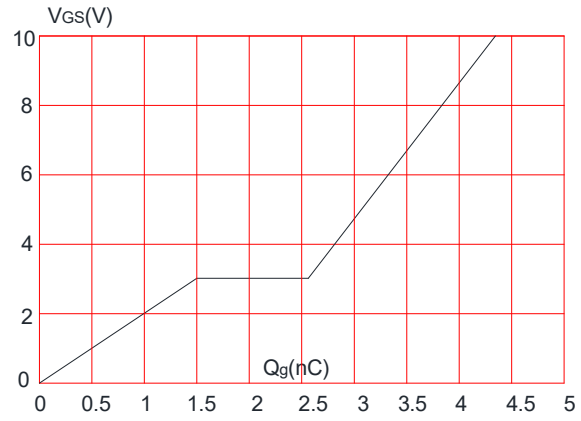


Figure 6: Capacitance Characteristics

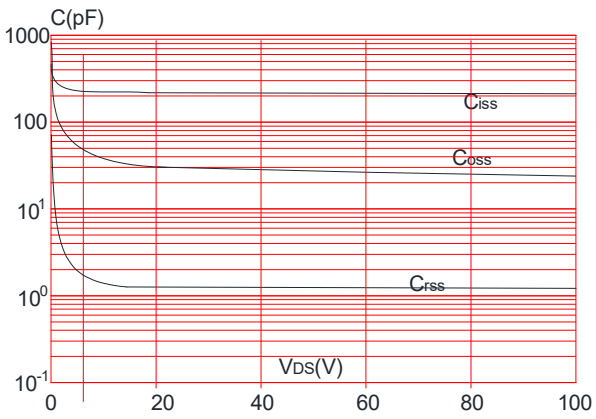


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

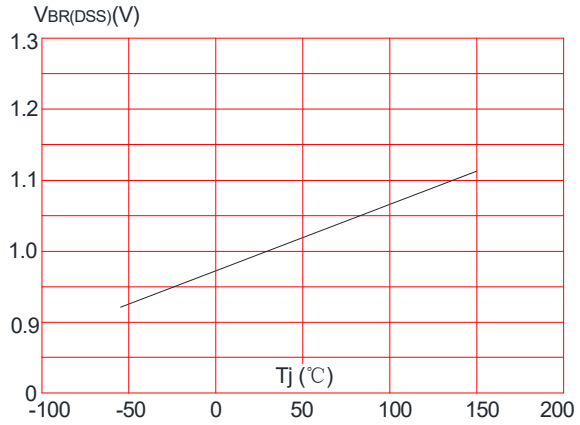


Figure 8: Normalized on Resistance vs. Junction Temperature

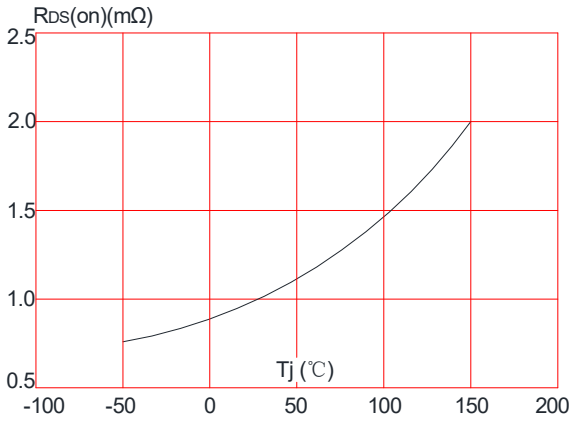


Figure 9: Maximum Safe Operating Area

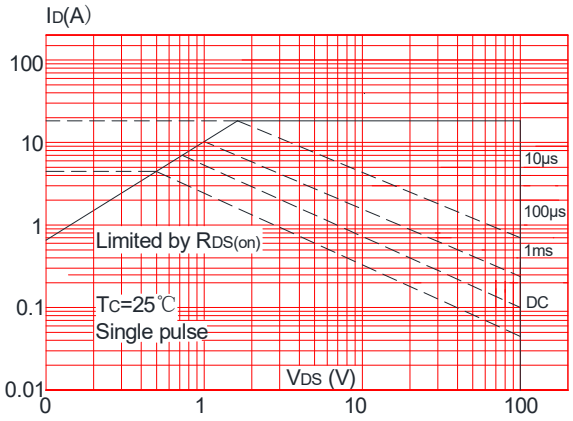


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

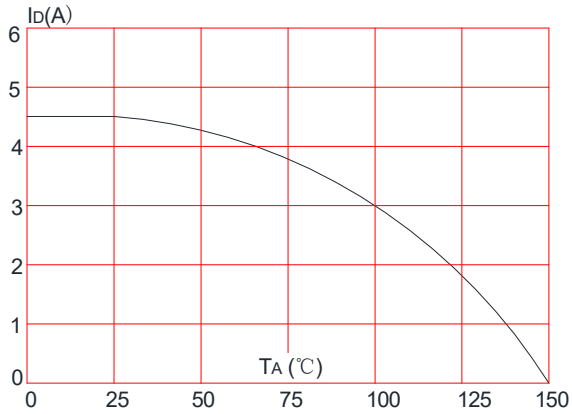
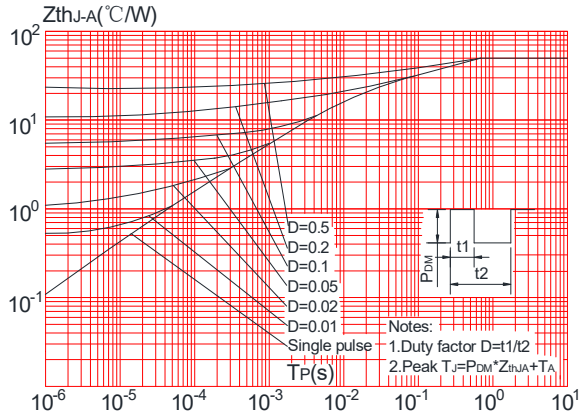


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



Test Circuit

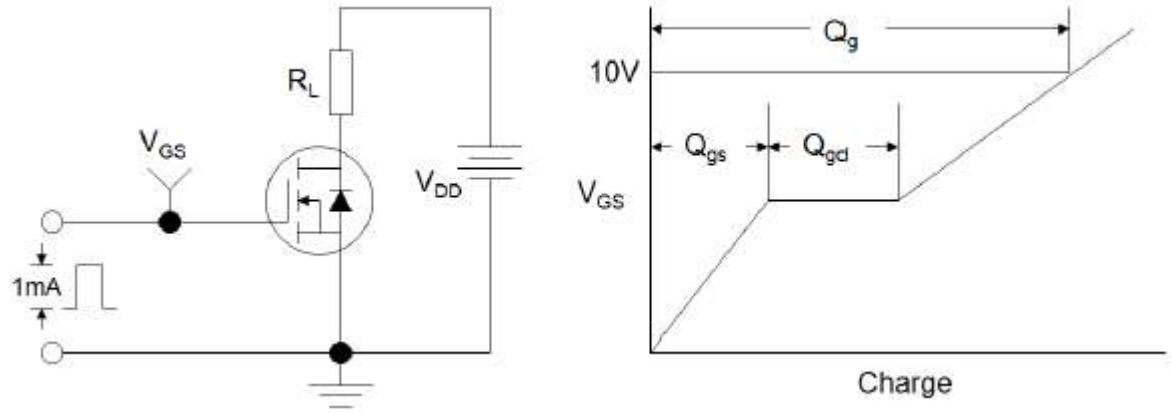


Figure1:Gate Charge Test Circuit & Waveform

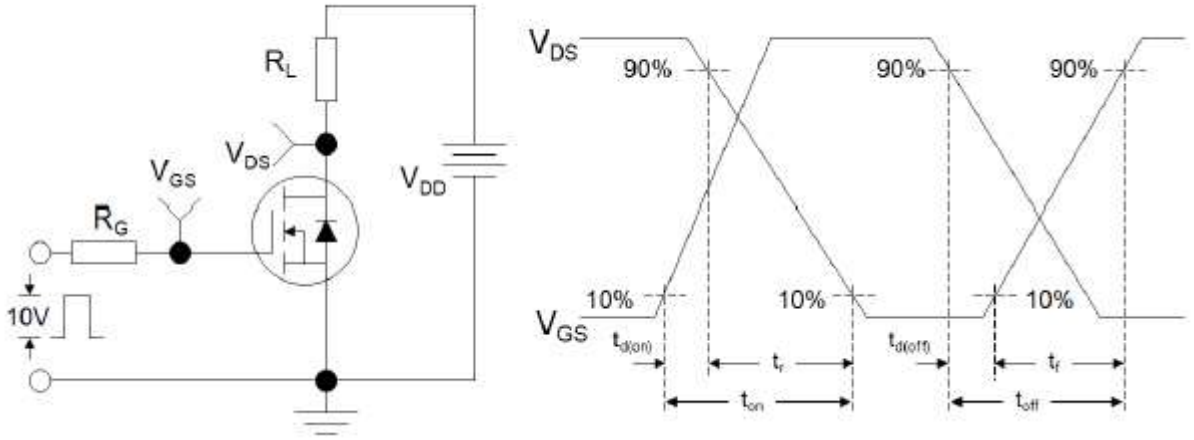


Figure 2: Resistive Switching Test Circuit & Waveforms

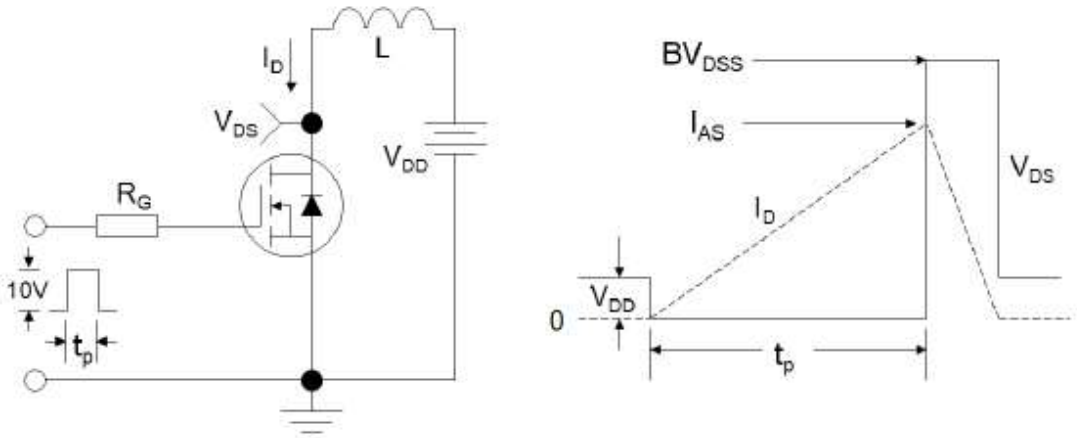


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

Package Mechanical Data-SOP-8