

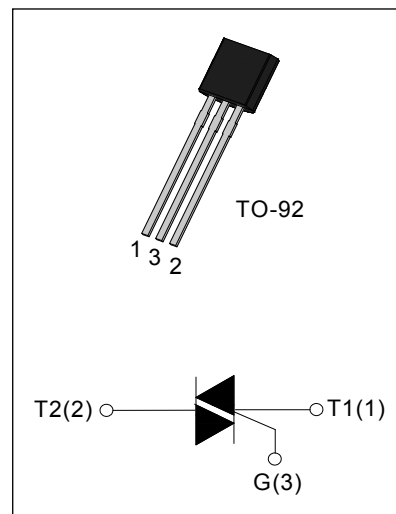


DESCRIPTION:

With low holding and latching current, JST130 series triacs are especially recommended for use on middle and small resistance type power load. Package TO-92 is RoHS compliant. (2011/65/EU)

MAIN FEATURES

Symbol	Value	Unit
$I_{T(RMS)}$	0.8	A
V_{TM}	1.5	V



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Storage junction temperature range	T_{stg}	-40 - 150	°C
Operating junction temperature range	T_j	-40 - 125	°C
Repetitive peak off-state voltage ($T_j=25^\circ\text{C}$)	V_{DRM}	600/800	V
Repetitive peak reverse voltage ($T_j=25^\circ\text{C}$)	V_{RRM}	600/800	V
RMS on-state current	$I_{T(RMS)}$	0.8	A
TO-92 ($T_c=50^\circ\text{C}$)			
Non repetitive surge peak on-state current (full cycle, F=50Hz)	I_{TSM}	9	A
I^2t value for fusing ($t_p=10\text{ms}$)	I^2t	0.45	A^2s
Critical rate of rise of on-state current ($I_G=2 \times I_{GT}$)	I - II - III	50	$\text{A}/\mu\text{s}$
	IV	20	
Peak gate current	I_{GM}	1	A
Average gate power dissipation	$P_{G(AV)}$	0.1	W
Peak gate power	P_{GM}	1	W

ELECTRICAL CHARACTERISTICS ($T_j=25^{\circ}\text{C}$ unless otherwise specified)

Symbol	Test Condition	Quadrant	Value		Unit	
			D	T		
I_{GT}	$V_D=12\text{V}$	I - II - III	MAX	5	5	mA
		IV		10	5	
V_{GT}		ALL	MAX	1.3		V
V_{GD}	$V_D=V_{DRM}$ $T_j=125^{\circ}\text{C}$ $R_L=3.3\text{K}\Omega$	ALL	MIN	0.2		V
I_L	$I_G=1.2I_{GT}$	I - III - IV	MAX	10	5	mA
		II		20	15	
I_H	$I_T=100\text{mA}$		MAX	7	5	mA
dV/dt	$V_D=2/3V_{DRM}$ Gate Open $T_j=125^{\circ}\text{C}$		MIN	30	10	V/ μs

STATIC CHARACTERISTICS

Symbol	Parameter		Value(MAX)	Unit
V_{TM}	$I_{TM}=1.1\text{A}$ $t_p=380\mu\text{s}$	$T_j=25^{\circ}\text{C}$	1.5	V
I_{DRM}	$V_D=V_{DRM}$ $V_R=V_{RRM}$	$T_j=25^{\circ}\text{C}$	5	μA
I_{RRM}		$T_j=125^{\circ}\text{C}$	100	μA

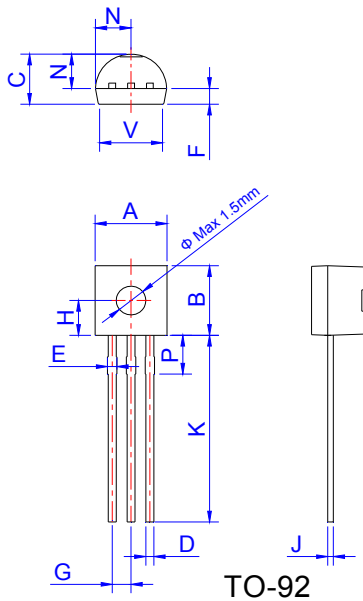
THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	junction to case(AC)	TO-92	75	$^{\circ}\text{C}/\text{W}$

ORDERING INFORMATION

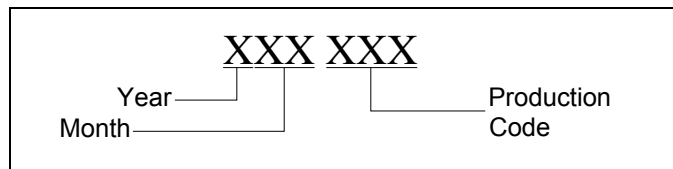
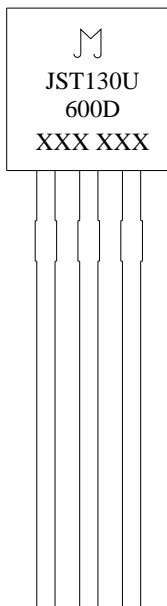
J	ST	130	U	-600	D
JieJie Microelectronics Co.,Ltd					
TRIACs					
$I_{T(RMS)}:0.8\text{A}$					
U:TO-92					
T: $I_{GT1-4}\leq 5\text{mA}$ D: $I_{GT1-3}\leq 5\text{mA}$ $I_{GT4}\leq 10\text{mA}$ 600: $V_{DRM}/V_{RRM}\geq 600\text{V}$ 800: $V_{DRM}/V_{RRM}\geq 800\text{V}$					

PACKAGE MECHANICAL DATA



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.45		5.20	0.175		0.205
B	4.32		5.33	0.170		0.210
C	3.18		4.19	0.125		0.165
D	0.407		0.533	0.016		0.021
E	0.50		0.70	0.020		0.028
F	-	1.1	-	-	0.043	-
G	-	1.27	-	-	0.050	-
H	-	2.30	-	-	0.091	-
J	0.36		0.50	0.014		0.020
K	12.70		15.0	0.500		0.591
N	2.04		2.66	0.080		0.105
P	1.86		2.06	0.073		0.081
V	-		4.3	-		0.169

MARKING



PACKAEG INFORMATION

PACKAGE	WEIGHT (PER PCS)	OUTLINE	BAG (PCS)	INNER BOX (PCS)	PER CARTON
TO-92	0.1894g	Shielding Bag	1,000	10,000	30,000
TO-92	0.1894g	Shielding Bag	1,000	10,000	50,000
TO-92	0.1894g	Shielding Bag	1,000	10,000	100,000

FIG.1: Maximum power dissipation versus RMS on-state current

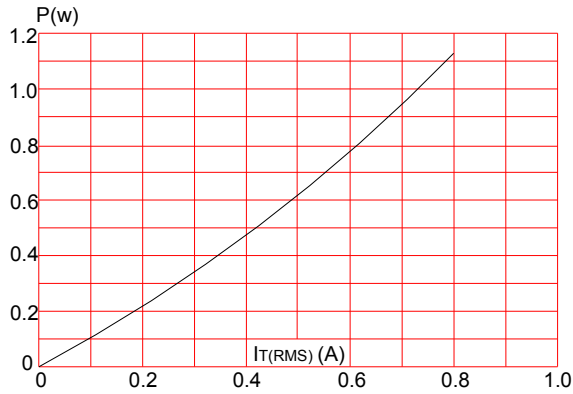


FIG.2: RMS on-state current versus case temperature

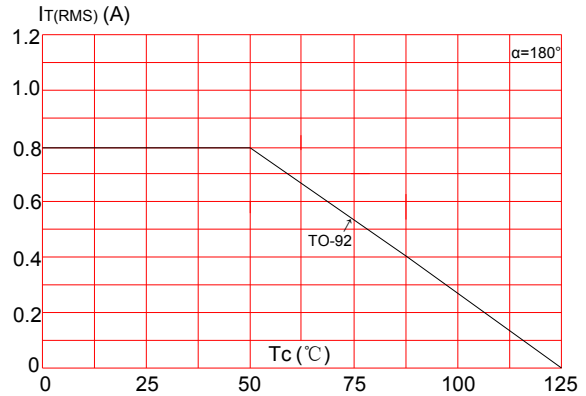


FIG.3: Surge peak on-state current versus number of cycles

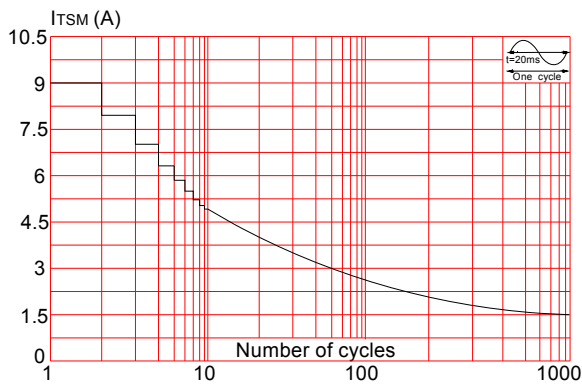


FIG.4: On-state characteristics (maximum values)

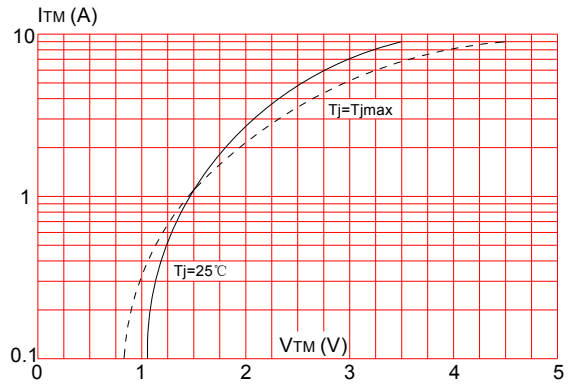


FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 20\text{ms}$ (I - II - III: $di/dt < 50\text{A}/\mu\text{s}$; IV: $di/dt < 20\text{A}/\mu\text{s}$)

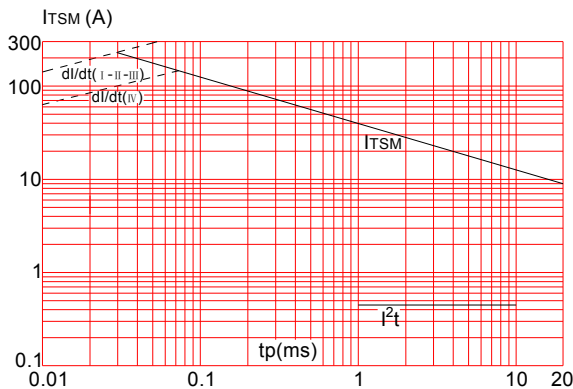
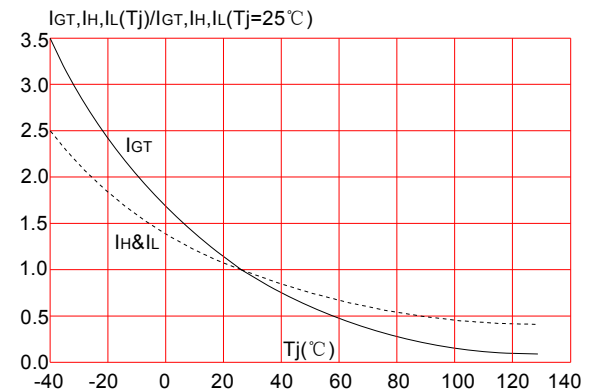



FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature



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