



Description

JMT Dual N-channel Enhancement Mode Power MOSFET

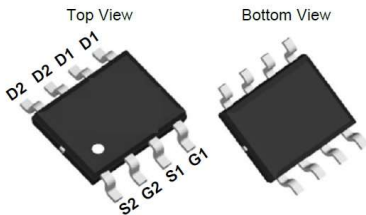
Features

- 20V, 6A
 $R_{DS(ON)} < 28m\Omega @ V_{GS} = 4.5V$
 $R_{DS(ON)} < 38m\Omega @ V_{GS} = 2.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

Application

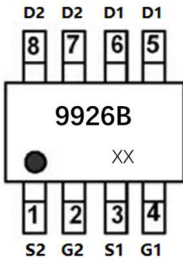
- Load Switch
- PWM Application
- Power management



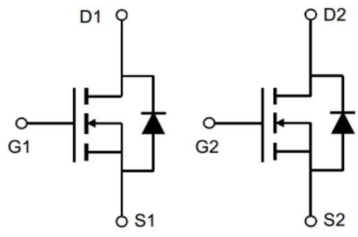


Top View Bottom View

SOP-8(Dual)



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
9926B	JMTP9926B	TAPING	SOP-8	13inch	4000	-

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise specified)

Symbol	Parameter	Max.	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	± 12	V
I_D	Continuous Drain Current	$T_A = 25^\circ C$	6
		$T_A = 100^\circ C$	4
I_{DM}	Pulsed Drain Current <small>note1</small>	24	A
P_D	Power Dissipation	$T_A = 25^\circ C$	1.6
$R_{\theta JA}$	Thermal Resistance, Junction to Case	78	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$



Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	20	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V,	-	-	1.0	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} =±12V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.4	0.7	1.0	V
R _{DS(on)}	Static Drain-Source on-Resistance <small>note2</small>	V _{GS} =4.5V, I _D =6A	-	20	28	mΩ
		V _{GS} =2.5V, I _D =5A	-	25.5	38	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =10V, V _{GS} =0V, f=1.0MHz	-	358	-	pF
C _{oss}	Output Capacitance		-	69.3	-	pF
C _{rss}	Reverse Transfer Capacitance		-	58.5	-	pF
Q _g	Total Gate Charge	V _{DS} =10V, I _D =3A, V _{GS} =4.5V	-	5.6	-	nC
Q _{gs}	Gate-Source Charge		-	0.8	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	1	-	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DS} =10V, I _D =6A, R _{GEN} =3Ω, V _{GS} =4.5V	-	16	-	ns
t _r	Turn-on Rise Time		-	51	-	ns
t _{d(off)}	Turn-off Delay Time		-	21	-	ns
t _f	Turn-off Fall Time		-	19	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	6	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	24	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S =6A	-	-	1.2	V

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%



Typical Performance Characteristics

Figure 1: Output Characteristics

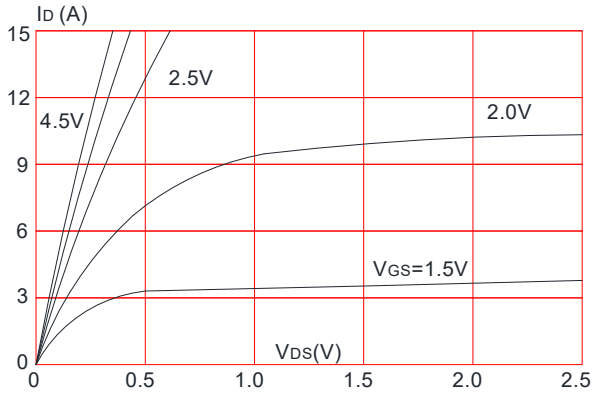


Figure 2: Typical Transfer Characteristics

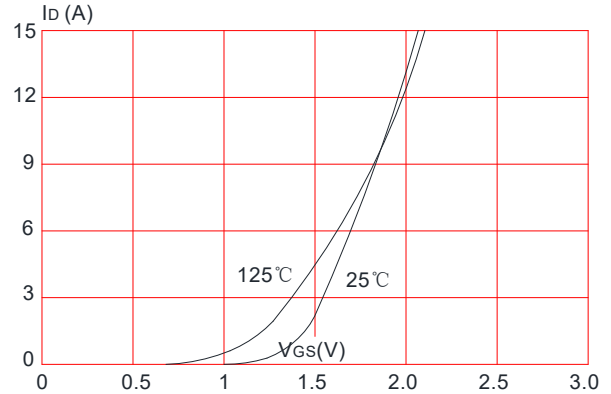


Figure 3: On-resistance vs. Drain Current

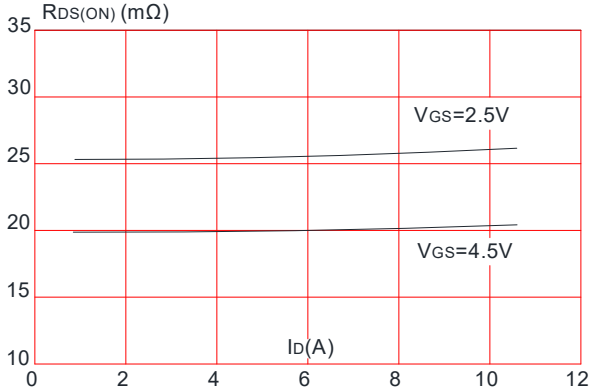


Figure 4: Body Diode Characteristics

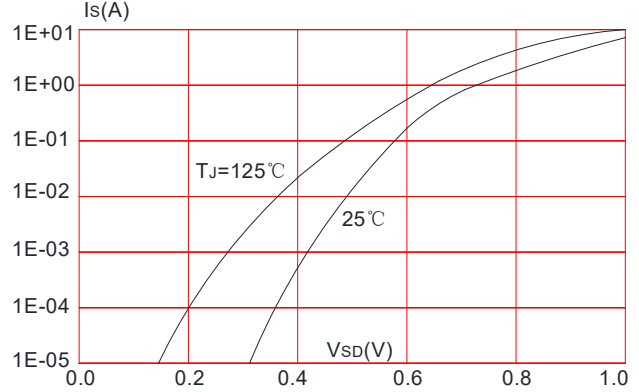


Figure 5: Gate Charge Characteristics

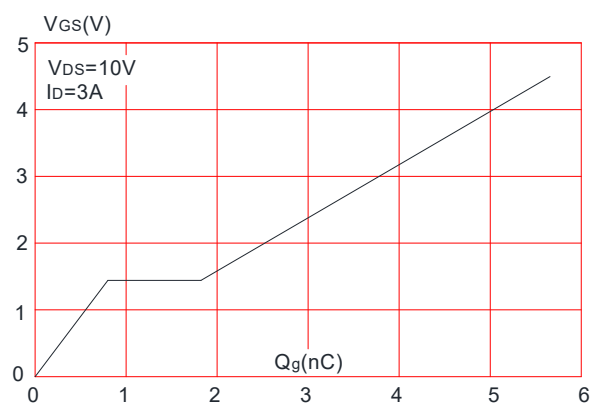


Figure 6: Capacitance Characteristics

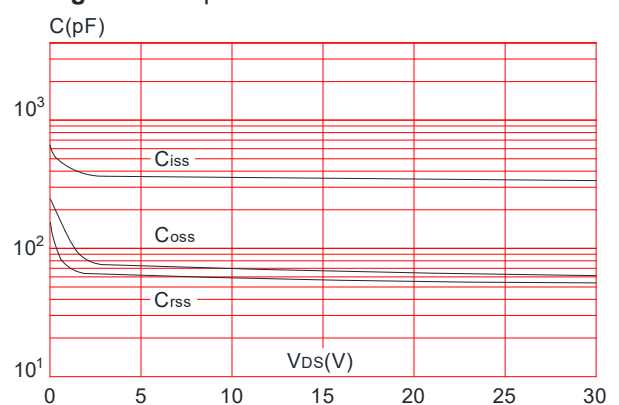




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

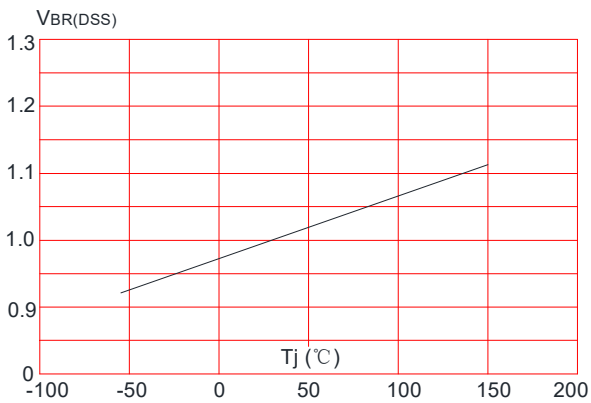


Figure 8: Normalized on Resistance vs. Junction Temperature

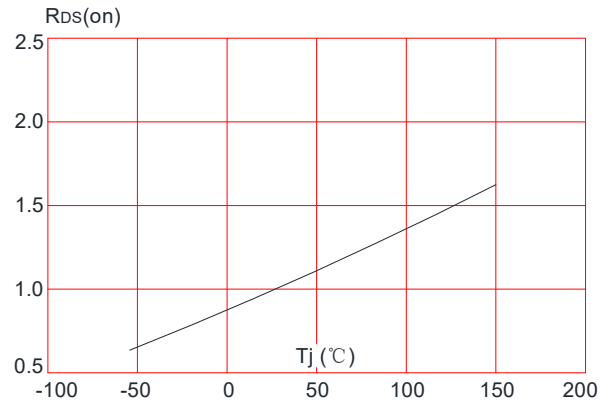


Figure 9: Maximum Safe Operating Area

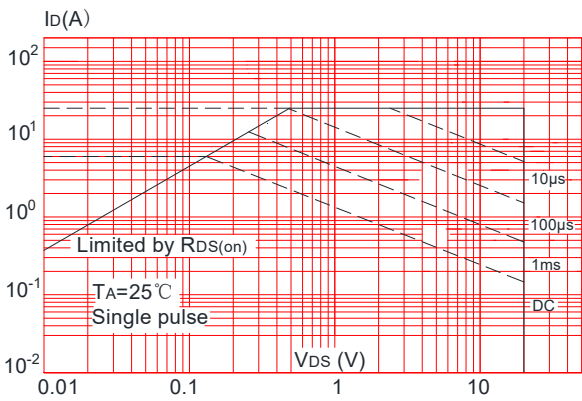


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

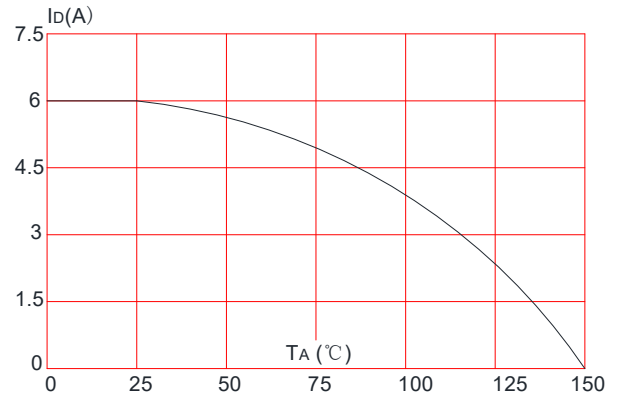
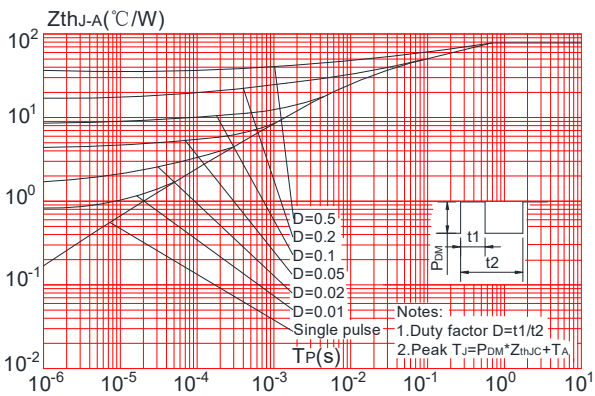


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



Test Circuit

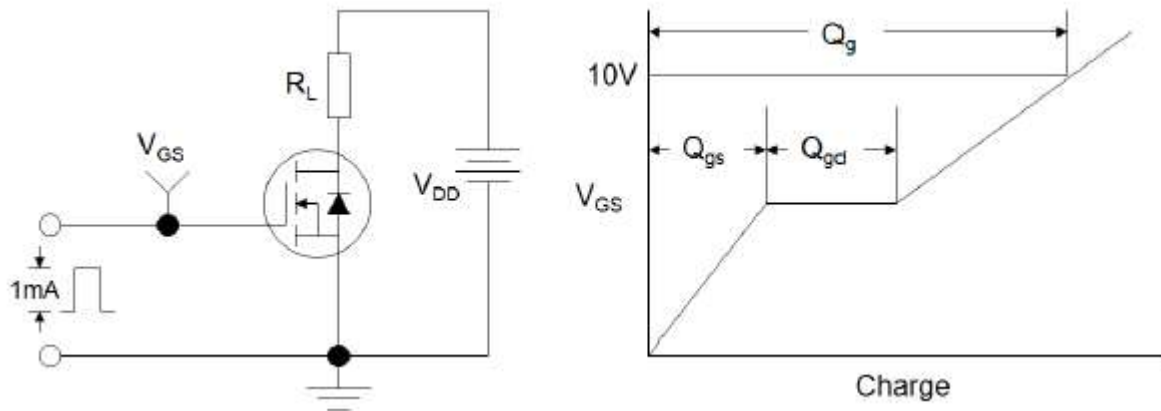


Figure1:Gate Charge Test Circuit & Waveform

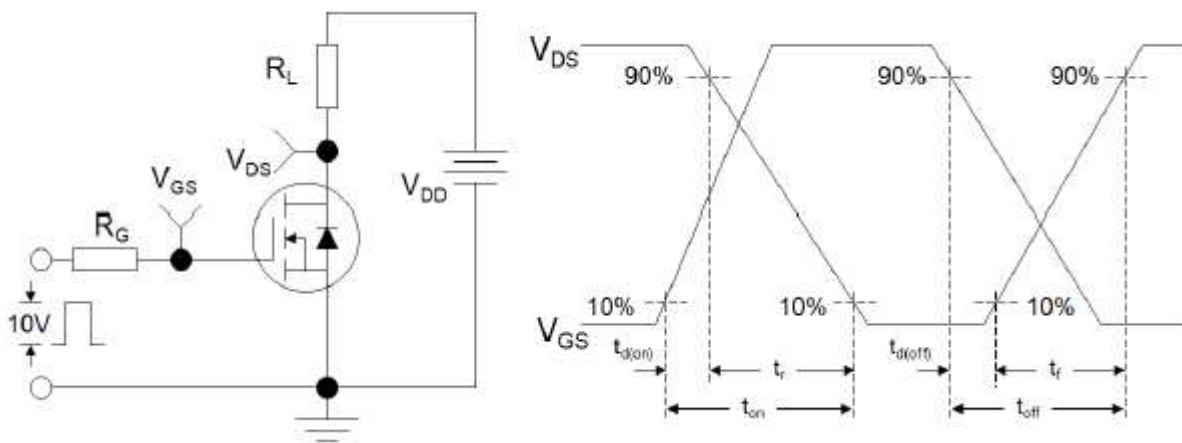


Figure 2: Resistive Switching Test Circuit & Waveforms

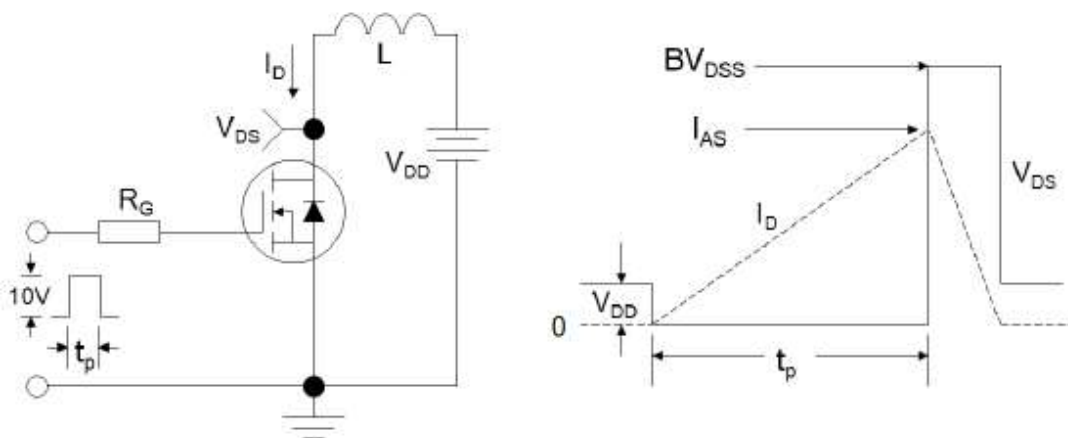
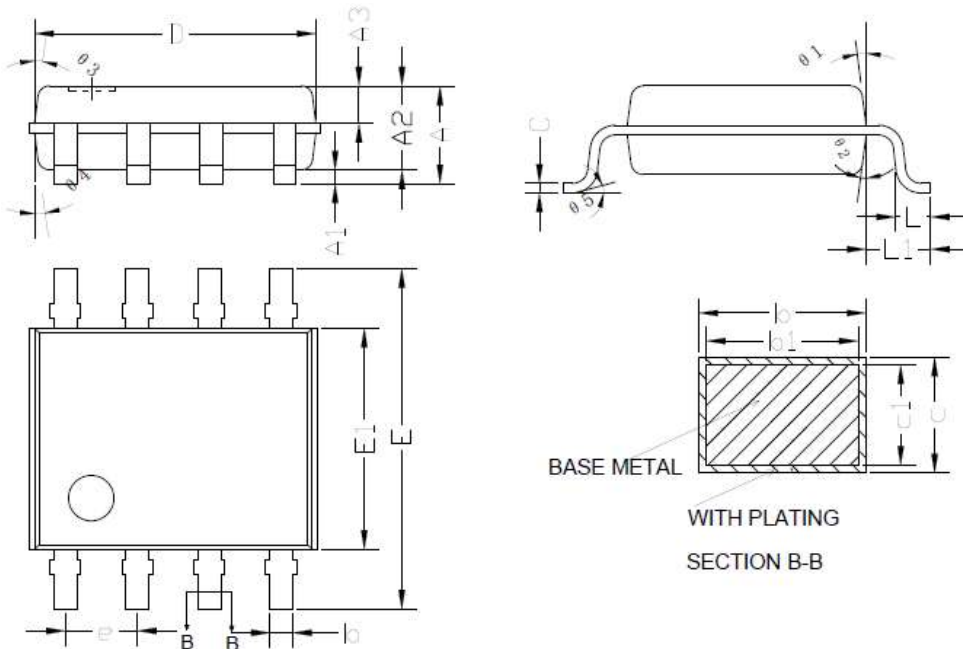


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



Package Mechanical Data-SOP-8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.65
A1	0.10	--	0.25
A2	1.40	1.42	1.50
A3	0.60	0.65	0.70
b	0.33	--	0.47
b1	0.32	0.41	0.44
c	0.20	--	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.90	6.00	6.20
E1	3.85	3.90	4.00
e	1.27(BSC)		
L	0.50	0.60	0.70
L1	1.05(BSC)		
θ_1	6°	~	12°
θ_2	6°	~	12°
θ_3	5°	~	10°
θ_4	5°	~	10°
θ_5	0°	~	6°

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